FIG. 1

(1)

1ST DATA a	0	1	0	1
1ST DATA b	0	0	1	1
2-BIT DATA	'00'	'01'	'10'	'11'

(2)

1ST OPERATION (a NAND b)	1	1	1	0
2ND OPERATION (NOT b)	1	1	0	0
3RD OPERATION (a NOR b)	1	0	0	0
NO. OF 1	3	2	1	0

(3)

DATA	THRESHOLD VALUE
'00'	V0 - 3Va
'01'	V0 - 2Va
'10'	V0 - Va
'11'	V0 (=ERASE LEVEL)

FIG. 2

c	0	0	0	1	(READ LEVEL: HIGHT)
d	0	0	1	1	(READ LEVEL: MEDIUM)
f	0	1	1	1	(READ LEVEL: LOW)
$\overline{d}$ NAND f	1	0	1	1	
($\overline{d}$ NAND f) NAND $\overline{c}$	0	1	0	1	= a
d	0	0	1	1	= b

FIG. 3

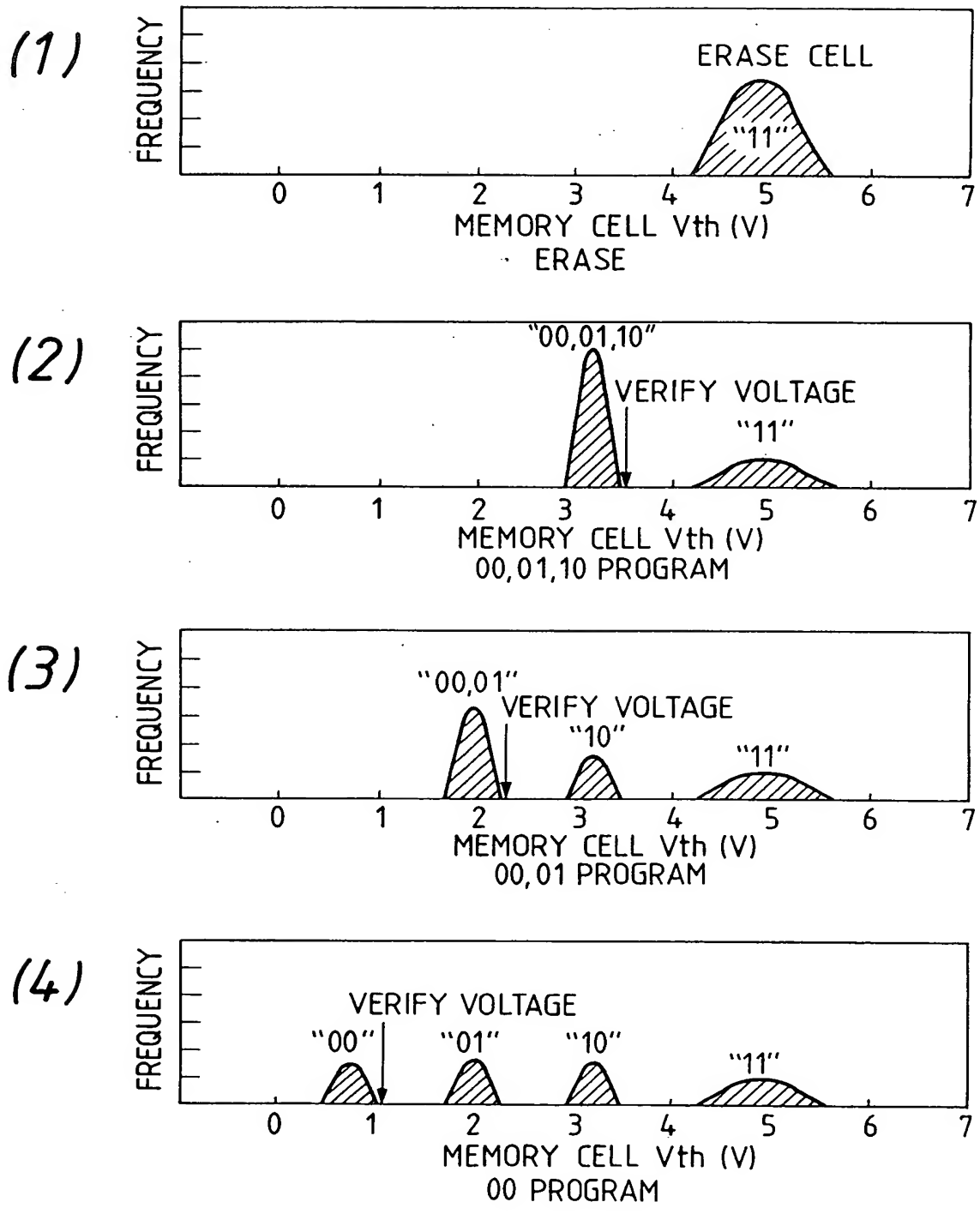

(1)
FREQUENCY
ERASE CELL
"11"
0 1 2 3 4 5 6 7
MEMORY CELL Vth (V)
ERASE
(2)
FREQUENCY
"00,01,10"
VERIFY VOLTAGE
"11"
0 1 2 3 4 5 6 7
MEMORY CELL Vth (V)
00,01,10 PROGRAM
(3)
FREQUENCY
"00,01"
VERIFY VOLTAGE
"10"
"11"
0 1 2 3 4 5 6 7
MEMORY CELL Vth (V)
00,01 PROGRAM
(4)
FREQUENCY
VERIFY VOLTAGE
"00"
"01"
"10"
"11"
0 1 2 3 4 5 6 7
MEMORY CELL Vth (V)
00 PROGRAM

FIG. 4

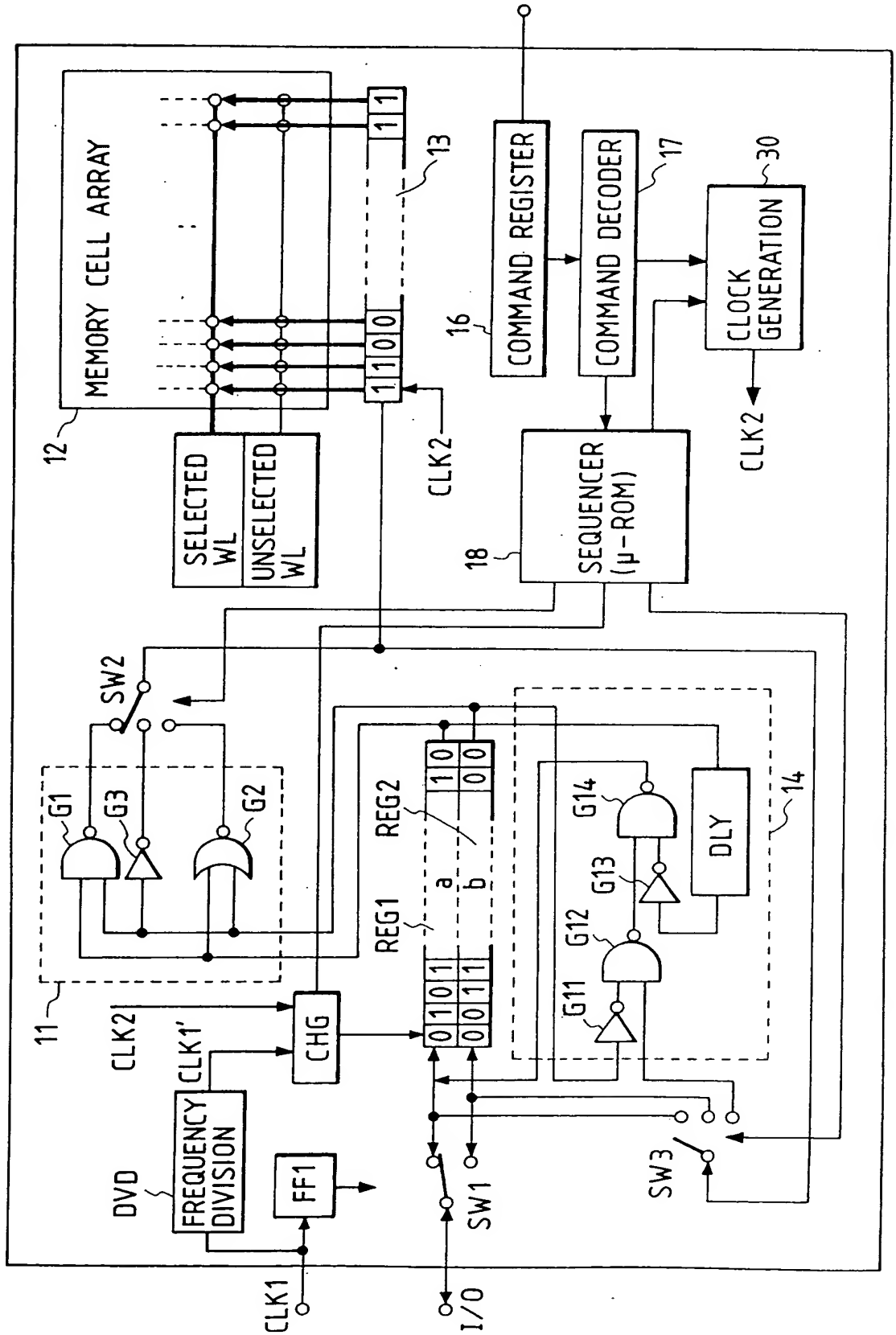

MEMORY CELL ARRAY
12
SELECTED WL
UNSELECTED WL
13
CLK2
COMMAND REGISTER
16
COMMAND DECODER
17
CLOCK GENERATION
30
CLK2
SEQUENCER (μ-ROM)
18
SW2
G1
G3
G2
REG2
REG1
a
b
G14
G13
G12
G11
DLY
14
11
CLK2
CLK1'
CHG
DVD
FREQUENCY DIVISION
FF1
CLK1
SW1
I/O
SW3

FIG. 5

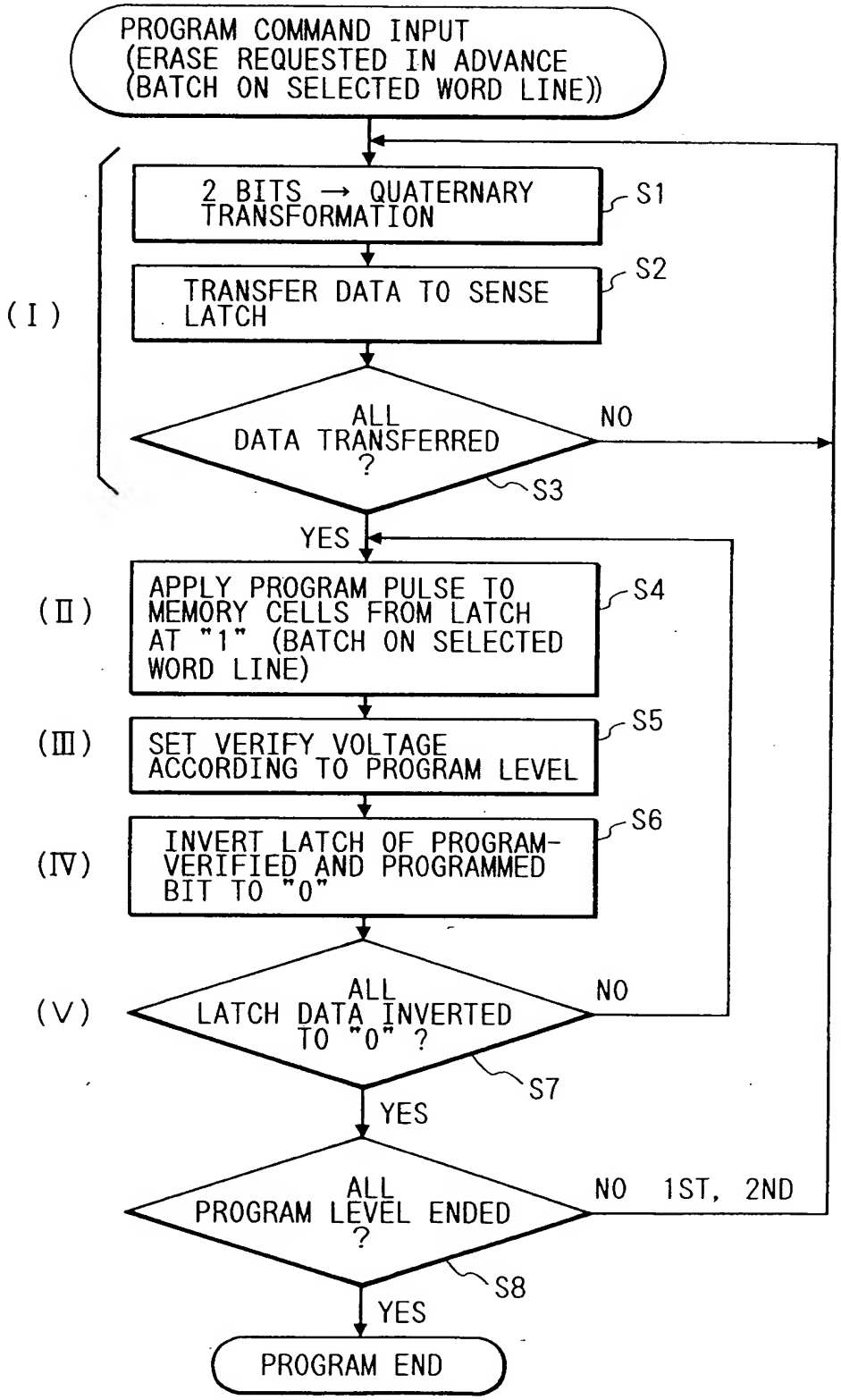

PROGRAM COMMAND INPUT
(ERASE REQUESTED IN ADVANCE
(BATCH ON SELECTED WORD LINE))
2 BITS → QUATERNARY TRANSFORMATION
S1
TRANSFER DATA TO SENSE LATCH
S2
(I)
ALL DATA TRANSFERRED ?
NO
S3
YES
APPLY PROGRAM PULSE TO MEMORY CELLS FROM LATCH AT "1" (BATCH ON SELECTED WORD LINE)
S4
(II)
SET VERIFY VOLTAGE ACCORDING TO PROGRAM LEVEL
S5
(III)
INVERT LATCH OF PROGRAM-VERIFIED AND PROGRAMMED BIT TO "0"
S6
(IV)
ALL LATCH DATA INVERTED TO "0" ?
NO
(V)
S7
YES
ALL PROGRAM LEVEL ENDED ?
NO 1ST, 2ND
S8
YES
PROGRAM END

FIG. 6

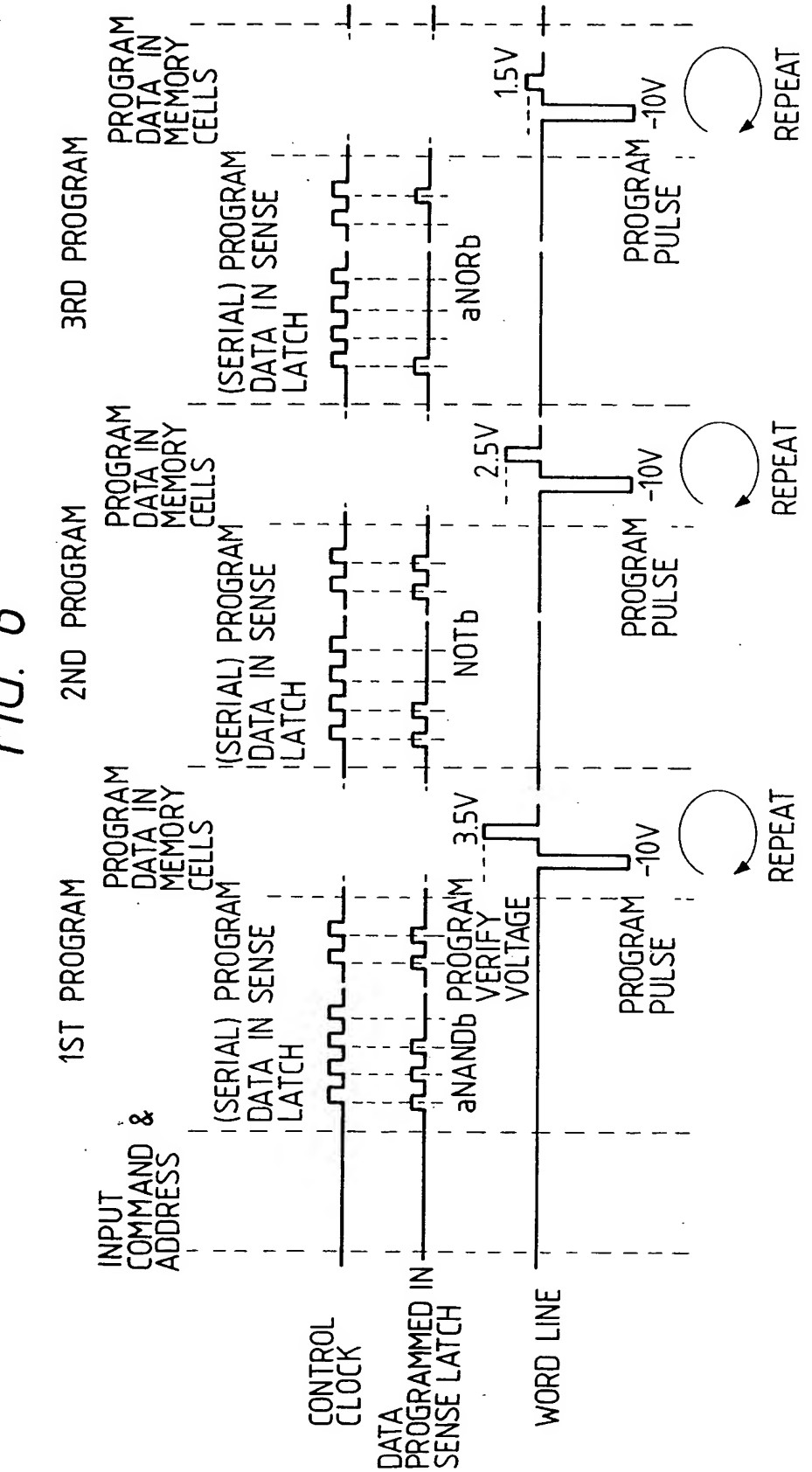

1ST PROGRAM
2ND PROGRAM
3RD PROGRAM
INPUT COMMAND & ADDRESS
(SERIAL) PROGRAM DATA IN SENSE LATCH
PROGRAM DATA IN MEMORY CELLS
aNANDb
NOTb
aNORb
PROGRAM VERIFY VOLTAGE
3.5V
2.5V
1.5V
PROGRAM PULSE
-10V
REPEAT
CONTROL CLOCK
DATA PROGRAMMED IN SENSE LATCH
WORD LINE

FIG. 7

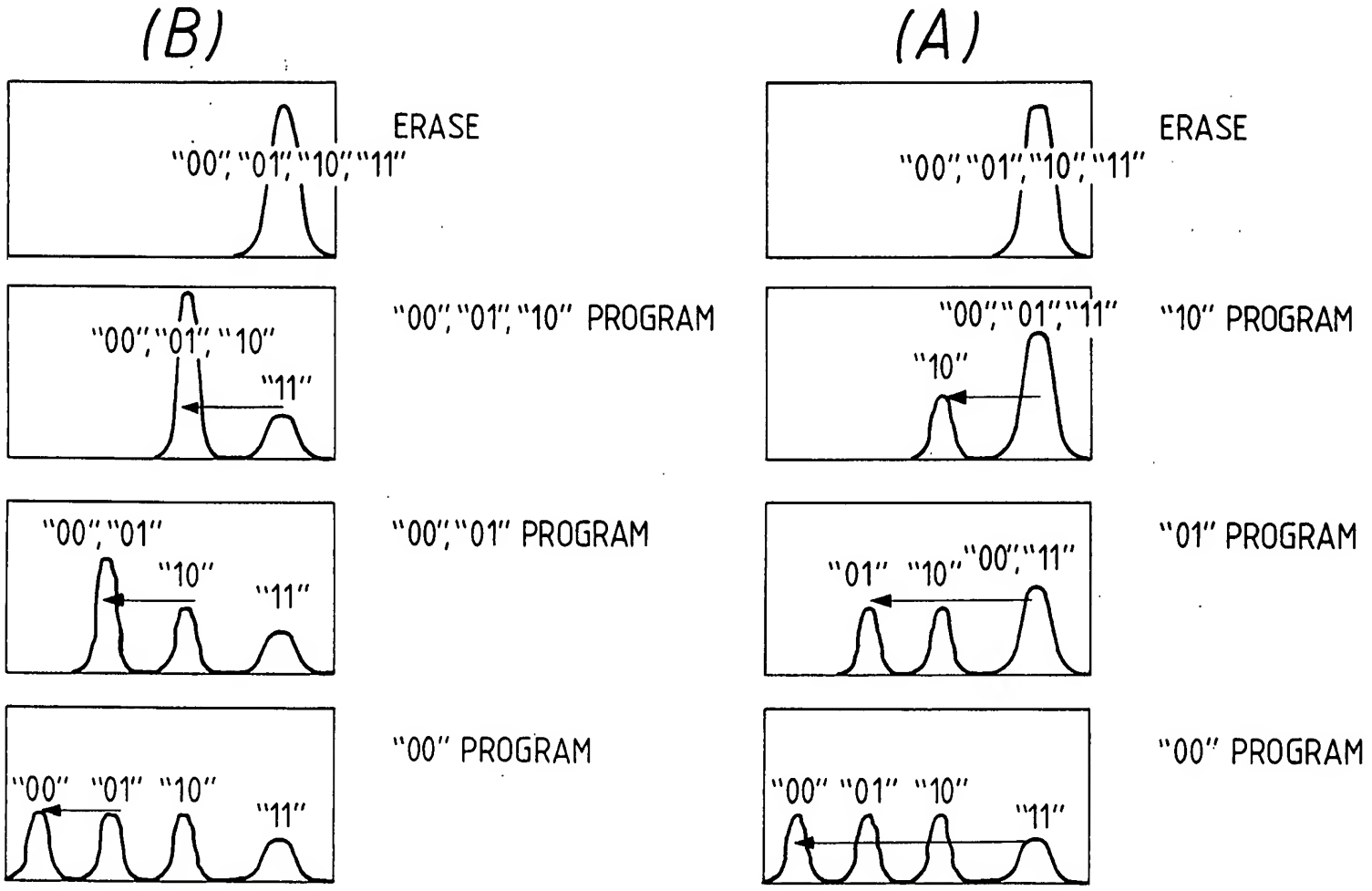

(B)
(A)
ERASE
"00", "01", "10", "11"
"00", "01", "10" PROGRAM
"10" PROGRAM
"00", "01"
"10"
"11"
"01" PROGRAM
"00" PROGRAM
1. BATCH OF PLURAL LEVELS
2. EACH UNIT LEVEL

FIG. 8

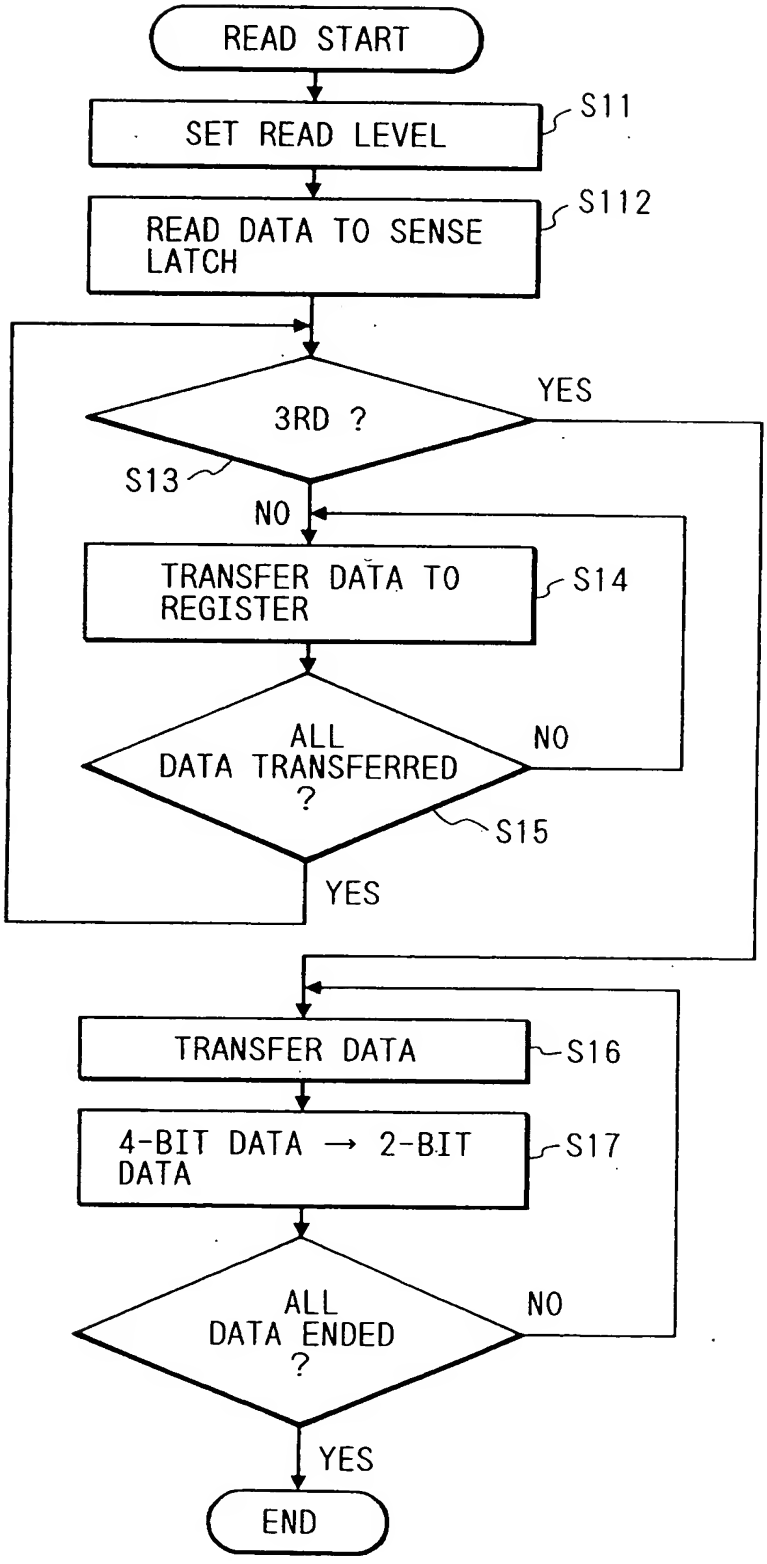

READ START
SET READ LEVEL
S11
READ DATA TO SENSE LATCH
S112
3RD ?
YES
S13
NO
TRANSFER DATA TO REGISTER
S14
ALL DATA TRANSFERRED ?
NO
S15
YES
TRANSFER DATA
S16
4-BIT DATA → 2-BIT DATA
S17
ALL DATA ENDED ?
NO
YES
END

FIG. 9

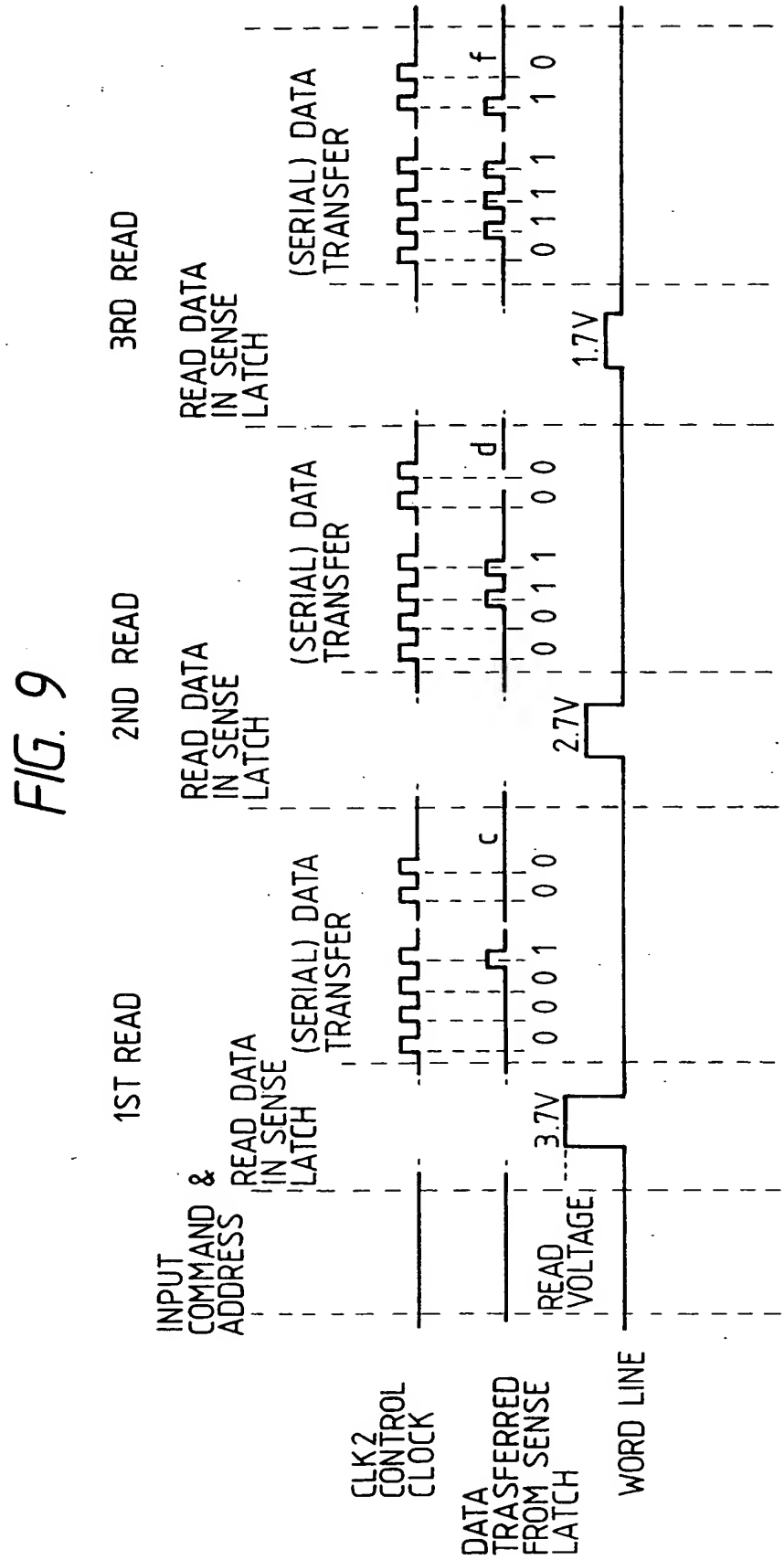

1ST READ
2ND READ
3RD READ
INPUT COMMAND & ADDRESS
READ DATA IN SENSE LATCH
(SERIAL) DATA TRANSFER
READ DATA IN SENSE LATCH
(SERIAL) DATA TRANSFER
READ DATA IN SENSE LATCH
(SERIAL) DATA TRANSFER
c
d
f
0 0 0 1 0 0
0 0 1 1 0 0
0 1 1 1 1 0
READ VOLTAGE
3.7V
2.7V
1.7V
CLK2 CONTROL CLOCK
DATA TRASFERRED FROM SENSE LATCH
WORD LINE

FIG. 10

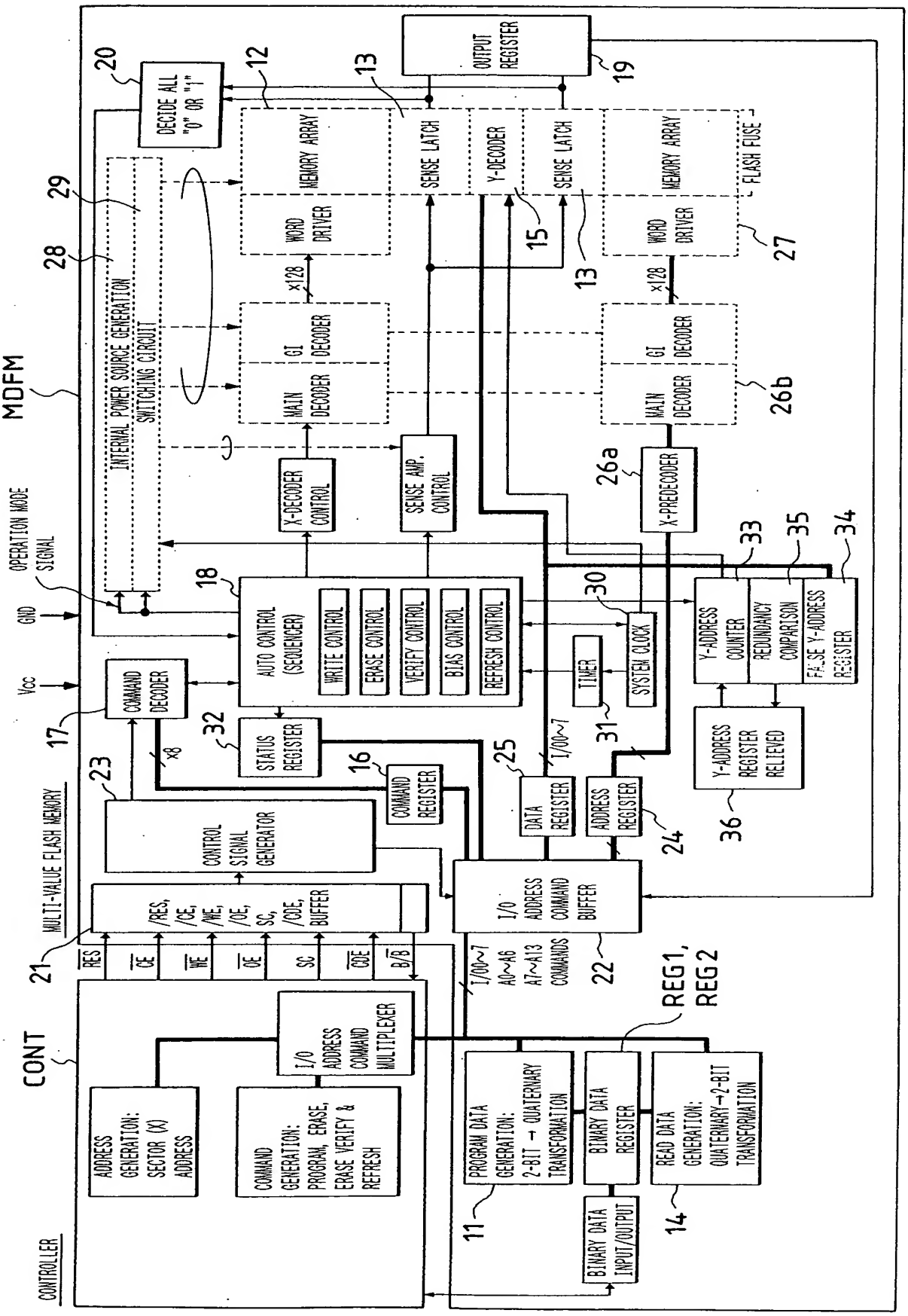

MDFM
MULTI-VALUE FLASH MEMORY
CONTROLLER
CONT
INTERNAL POWER SOURCE GENERATION SWITCHING CIRCUIT
DECIDE ALL "0" OR "1"
OUTPUT REGISTER
MEMORY ARRAY
WORD DRIVER
SENSE LATCH
Y-DECODER
FLASH FUSE
MAIN DECODER
GI DECODER
X-DECODER CONTROL
SENSE AMP. CONTROL
X-PREDECODER
OPERATION MODE SIGNAL
GND
Vcc
COMMAND DECODER
AUTO CONTROL (SEQUENCER)
WRITE CONTROL
ERASE CONTROL
VERIFY CONTROL
BIAS CONTROL
REFRESH CONTROL
TIMER
SYSTEM CLOCK
Y-ADDRESS COUNTER
REDUNDANCY COMPARISON
FALSE Y-ADDRESS REGISTER
STATUS REGISTER
COMMAND REGISTER
DATA REGISTER
ADDRESS REGISTER
Y-ADDRESS REGISTER RELIEVED
CONTROL SIGNAL GENERATOR
/RES, /OE, /WE, /OE, SC, /CDE, BUFFER
I/O ADDRESS COMMAND BUFFER
I/O ADDRESS COMMAND MULTIPLEXER
ADDRESS GENERATION: SECTOR (X) ADDRESS
COMMAND GENERATION: PROGRAM, ERASE, ERASE VERIFY & REFRESH
PROGRAM DATA GENERATION: 2-BIT → QUATERNARY TRANSFORMATION
BINARY DATA REGISTER
READ DATA GENERATION: QUATERNARY→2-BIT TRANSFORMATION
BINARY DATA INPUT/OUTPUT
REG1, REG2
I/O0~7
A0~A6
A7~A13
COMMANDS
RES
OE
WE
SC
CDE
B/B
x8
x128

FIG. 11

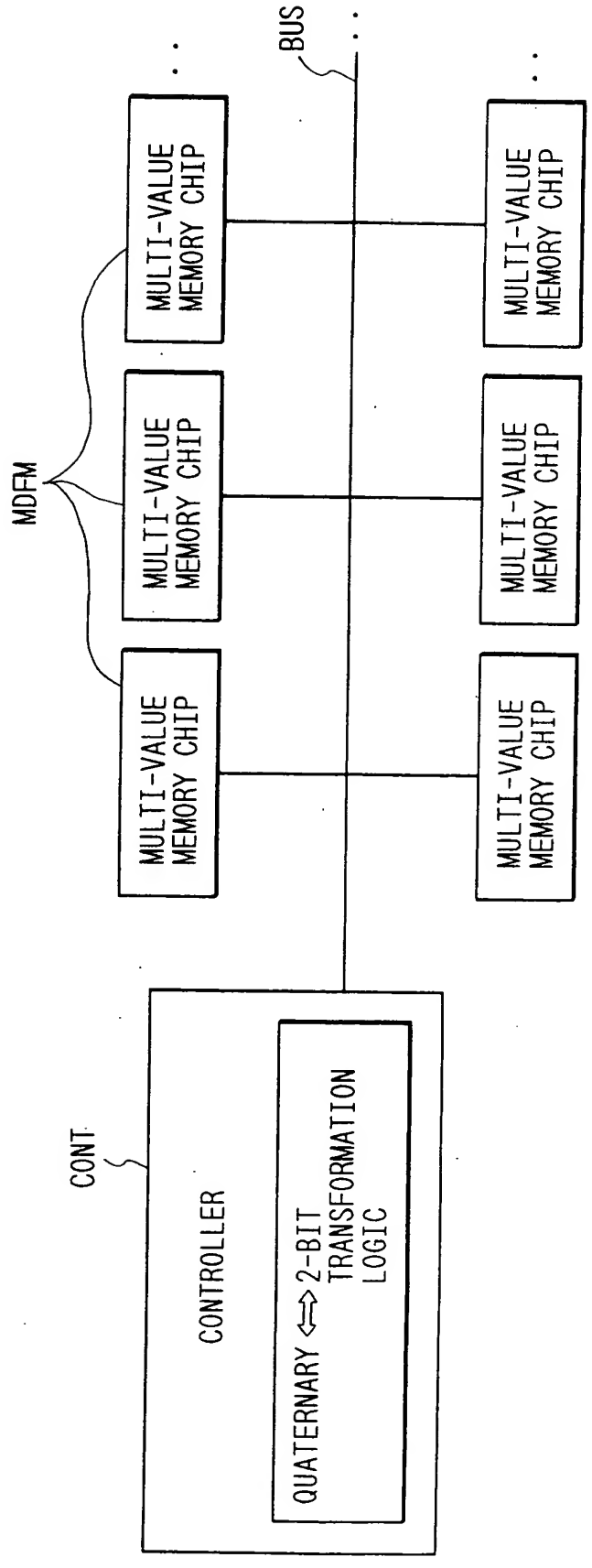
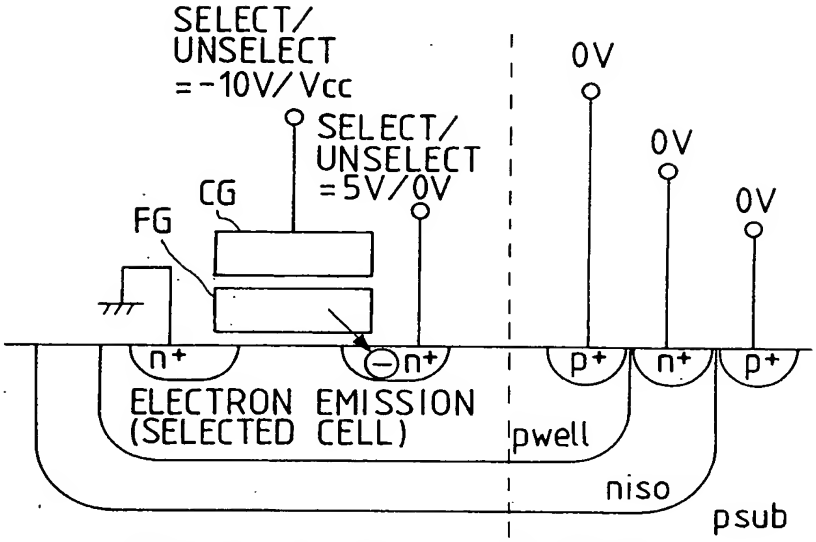
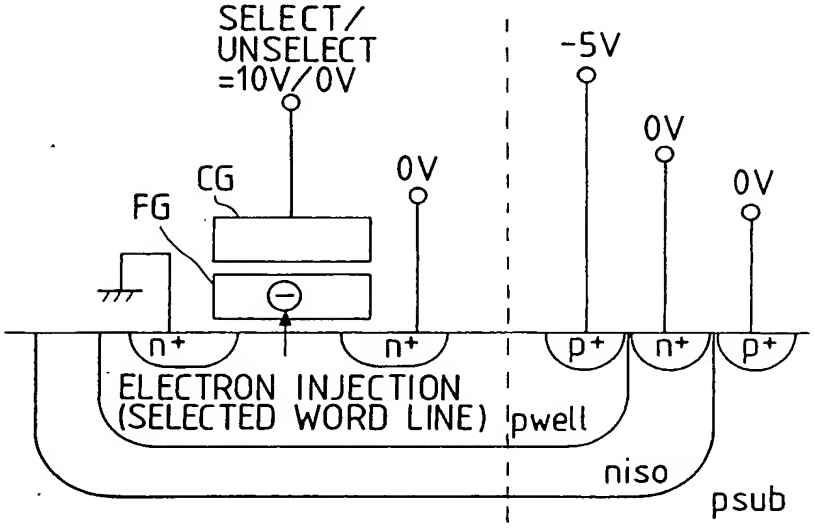

BUS
MDFM
MULTI-VALUE MEMORY CHIP
MULTI-VALUE MEMORY CHIP
MULTI-VALUE MEMORY CHIP
MULTI-VALUE MEMORY CHIP
MULTI-VALUE MEMORY CHIP
MULTI-VALUE MEMORY CHIP
CONT
CONTROLLER
QUATERNARY ⟺ 2-BIT TRANSFORMATION LOGIC

FIG. 12



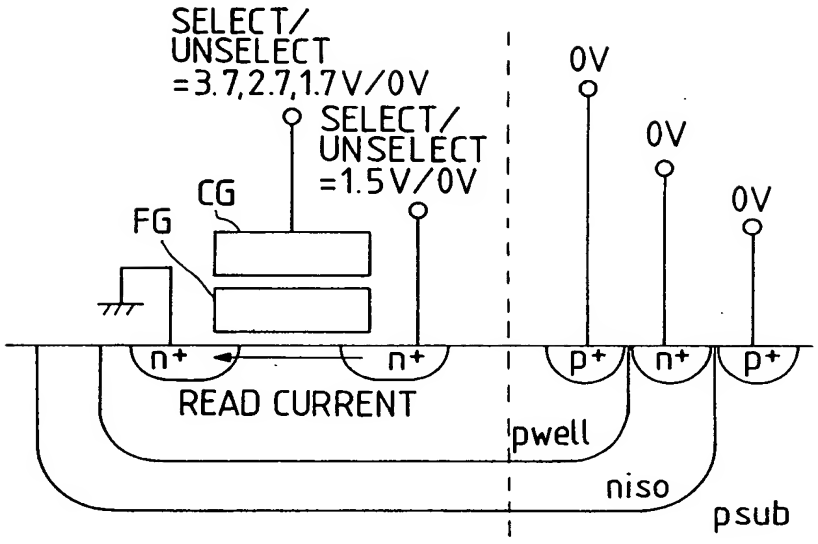
EXAMPLE OF APPLIED VOLTAGES
AT PROGRAMMING TIME

FIG. 13



EXAMPLE OF APPLIED VOLTAGES
AT ERASING TIME

FIG. 14



EXAMPLE OF APPLIED VOLTAGES AT READING TIME

FIG. 15

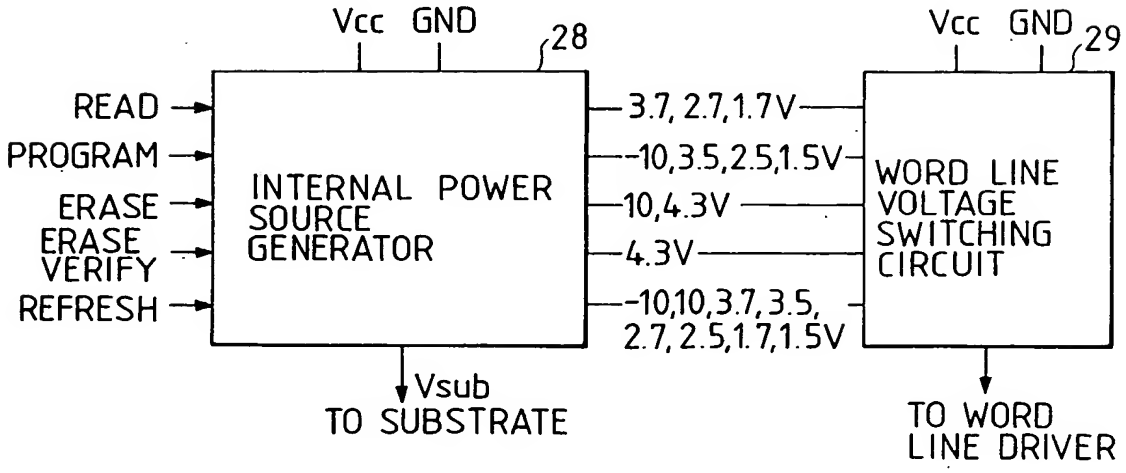


FIG. 16

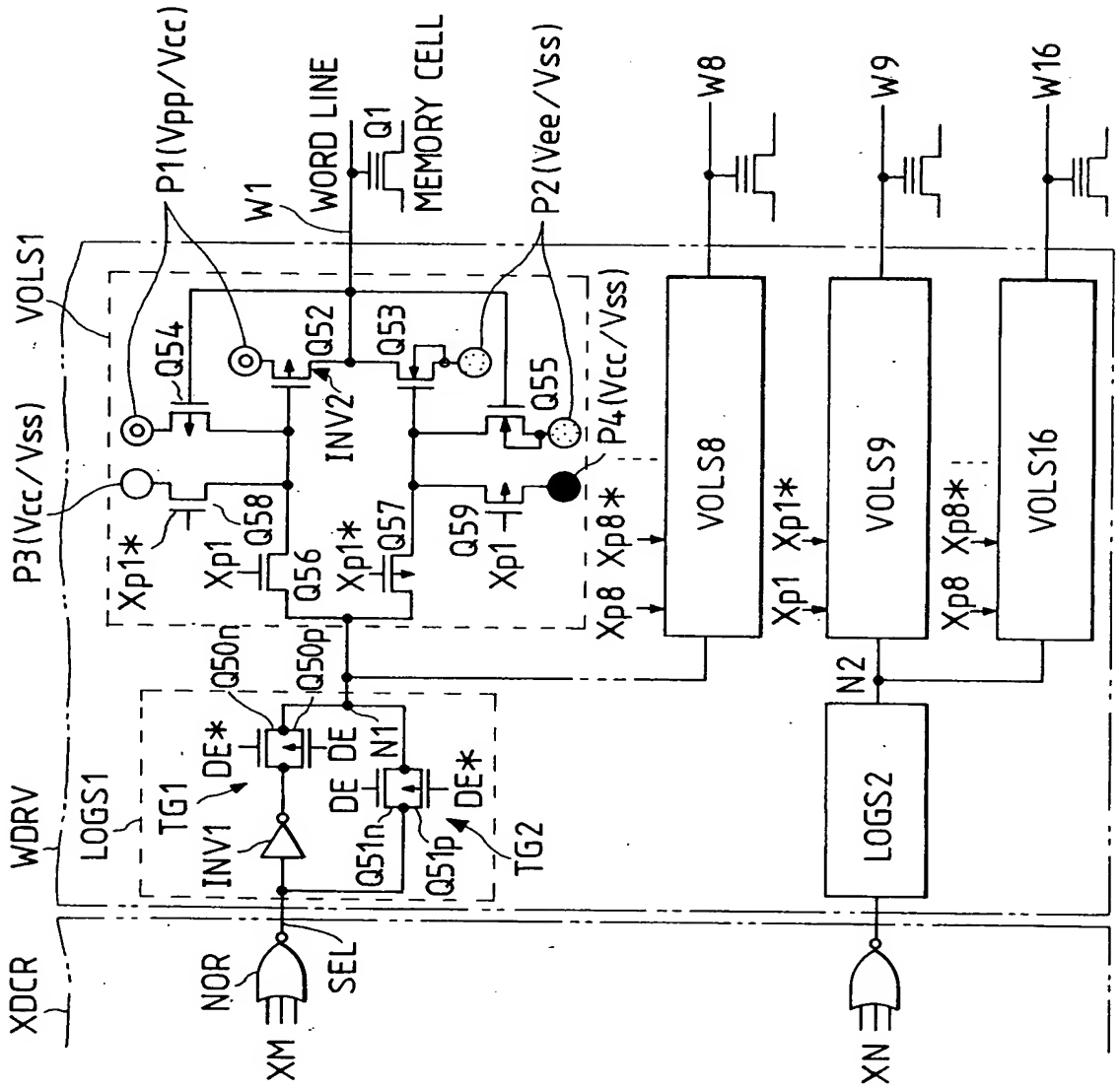

P1(Vpp/Vcc)
W1
WORD LINE
Q1
MEMORY CELL
P2(Vee/Vss)
W8
W9
W16
VOLS1
Q54
Q52
Q53
Q55
INV2
P3(Vcc/Vss)
P4(Vcc/Vss)
Xp1*
Xp1
Q58
Q56
Xp1*
Q57
Q59
Xp1
Xp8
Xp8*
VOLS8
VOLS9
VOLS16
Xp1
Xp1*
Xp8
Xp8*
Q50n
Q50p
N2
WDRV
LOGS1
TG1
DE*
DE
DE
N1
INV1
Q51n
Q51p
DE*
TG2
LOGS2
XDCR
NOR
SEL
XM
XN

FIG. 17

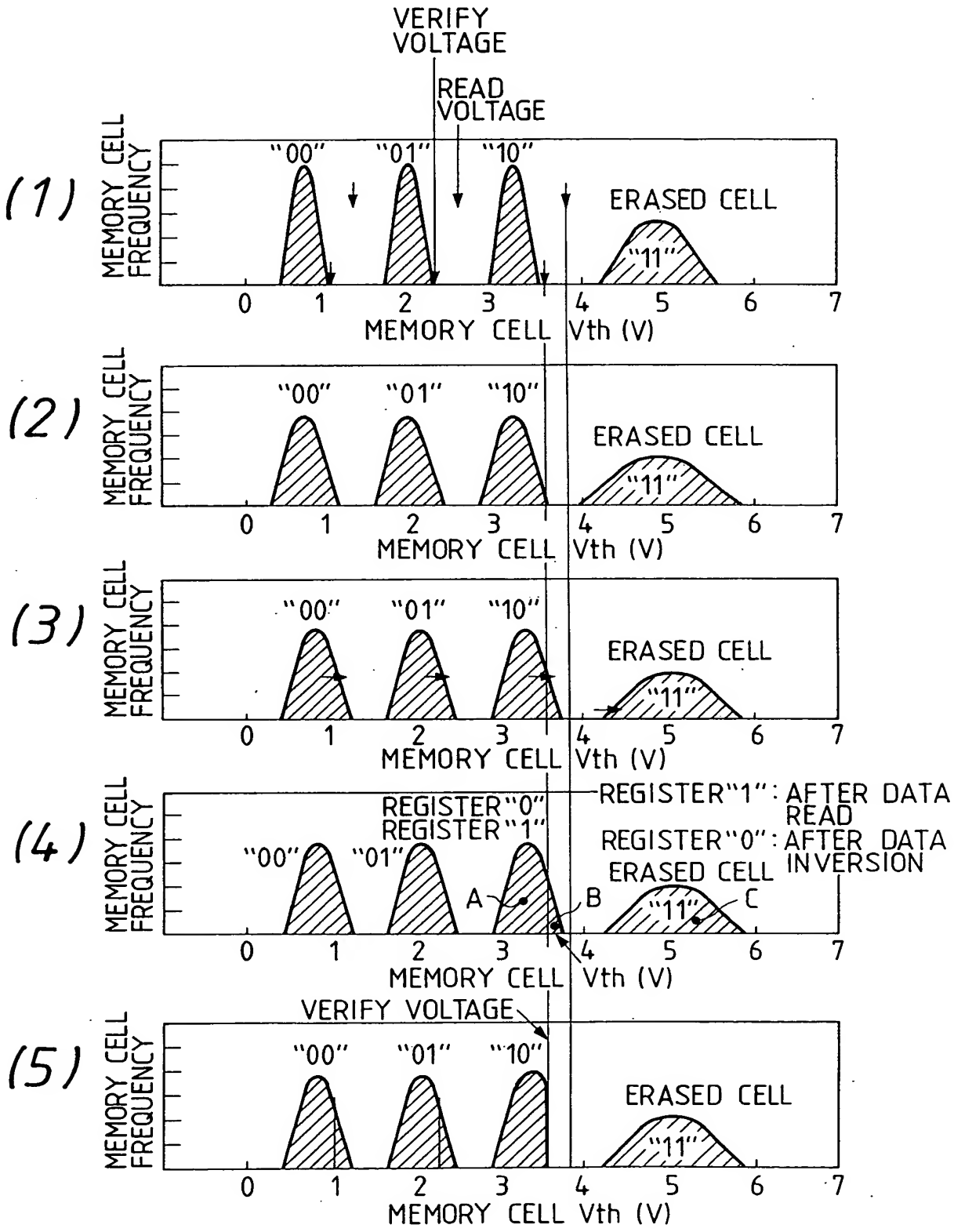

VERIFY VOLTAGE
READ VOLTAGE
(1)
(2)
(3)
(4)
(5)
MEMORY CELL FREQUENCY
"00"
"01"
"10"
"11"
ERASED CELL
0 1 2 3 4 5 6 7
MEMORY CELL Vth (V)
REGISTER"0"
REGISTER"1"
REGISTER"1": AFTER DATA READ
REGISTER"0": AFTER DATA INVERSION
A
B
C

FIG. 18

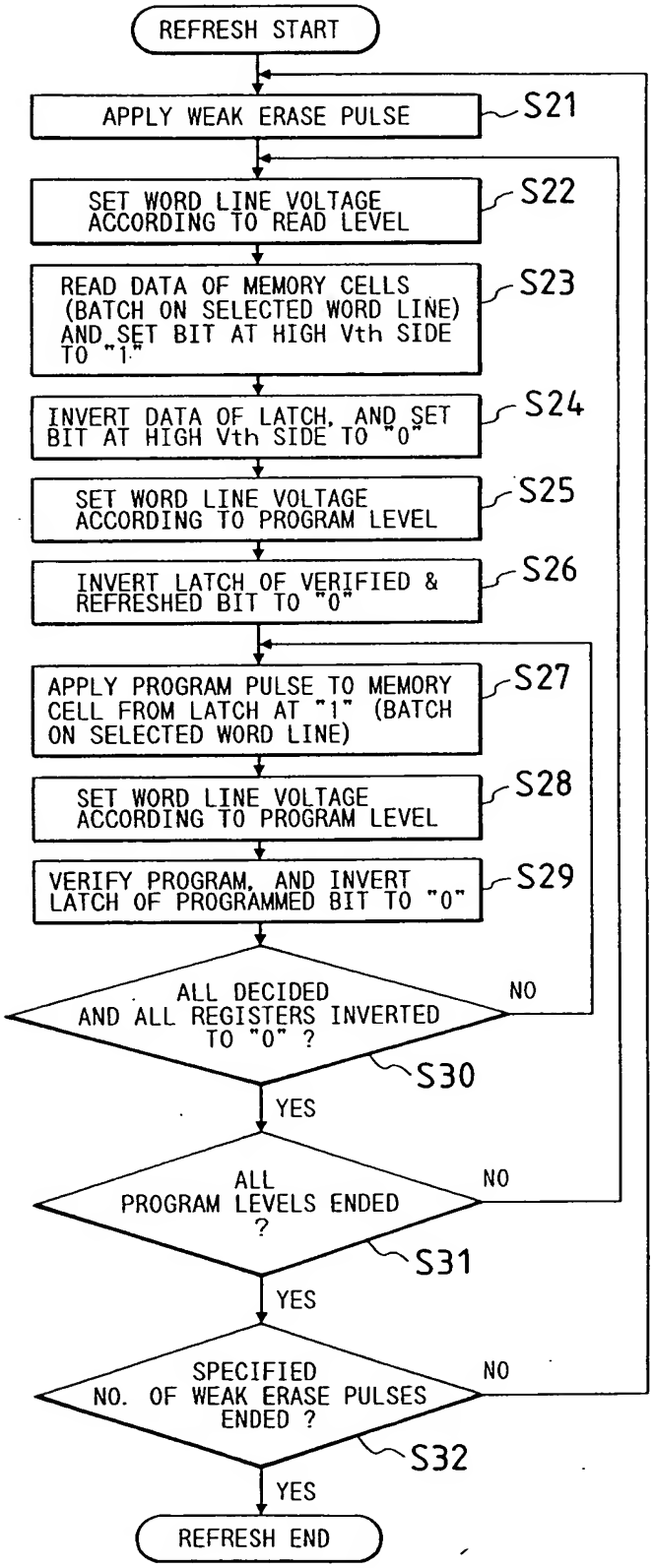

REFRESH START
APPLY WEAK ERASE PULSE
S21
SET WORD LINE VOLTAGE ACCORDING TO READ LEVEL
S22
READ DATA OF MEMORY CELLS (BATCH ON SELECTED WORD LINE) AND SET BIT AT HIGH Vth SIDE TO "1"
S23
INVERT DATA OF LATCH, AND SET BIT AT HIGH Vth SIDE TO "0"
S24
SET WORD LINE VOLTAGE ACCORDING TO PROGRAM LEVEL
S25
INVERT LATCH OF VERIFIED & REFRESHED BIT TO "0"
S26
APPLY PROGRAM PULSE TO MEMORY CELL FROM LATCH AT "1" (BATCH ON SELECTED WORD LINE)
S27
SET WORD LINE VOLTAGE ACCORDING TO PROGRAM LEVEL
S28
VERIFY PROGRAM, AND INVERT LATCH OF PROGRAMMED BIT TO "0"
S29
ALL DECIDED AND ALL REGISTERS INVERTED TO "0" ?
NO
S30
YES
ALL PROGRAM LEVELS ENDED ?
NO
S31
YES
SPECIFIED NO. OF WEAK ERASE PULSES ENDED ?
NO
S32
YES
REFRESH END

FIG. 19

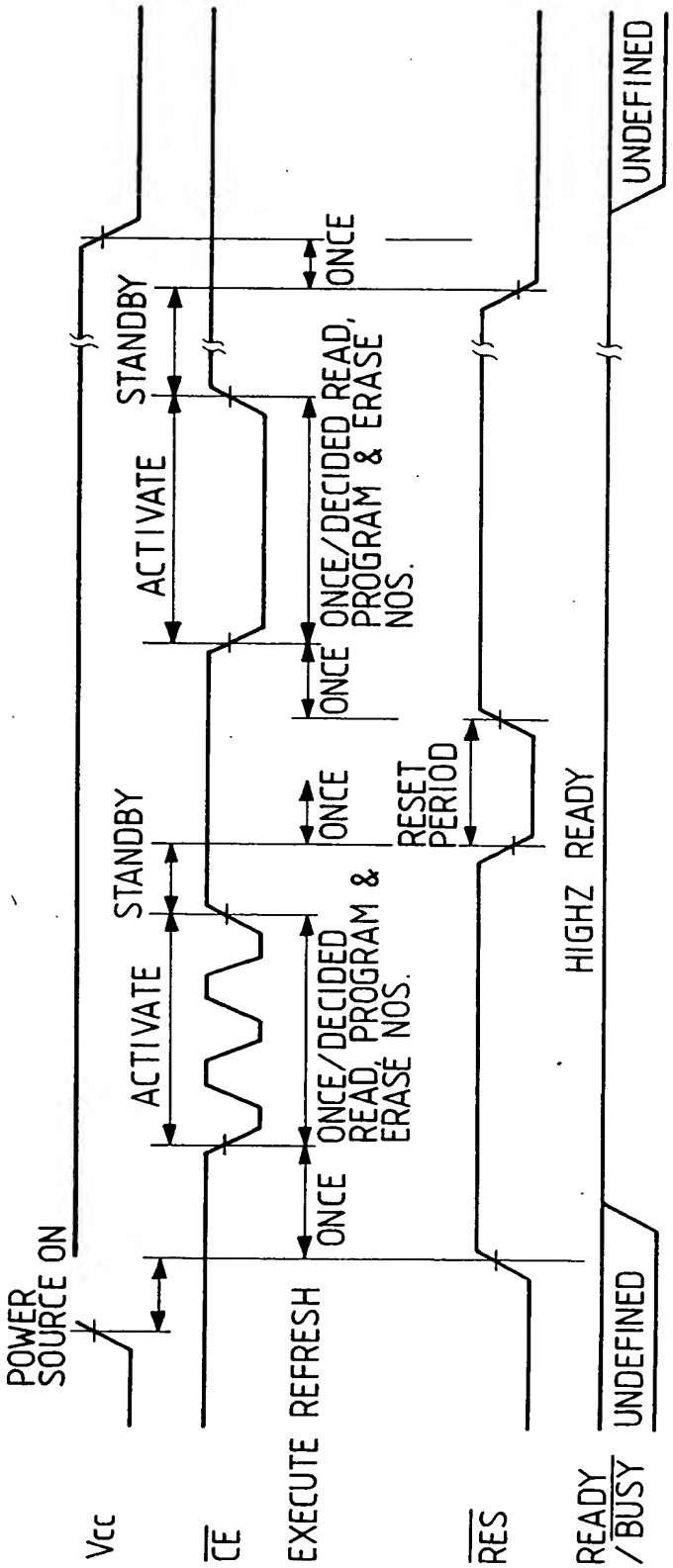

Vcc
CE
EXECUTE REFRESH
RES
READY /BUSY
POWER SOURCE ON
UNDEFINED
ACTIVATE
STANDBY
ONCE/DECIDED READ, PROGRAM & ERASE NOS.
ONCE
ONCE
ACTIVATE
STANDBY
ONCE/DECIDED READ, PROGRAM & ERASE NOS.
ONCE
RESET PERIOD
HIGHZ
READY
UNDEFINED

FIG. 20

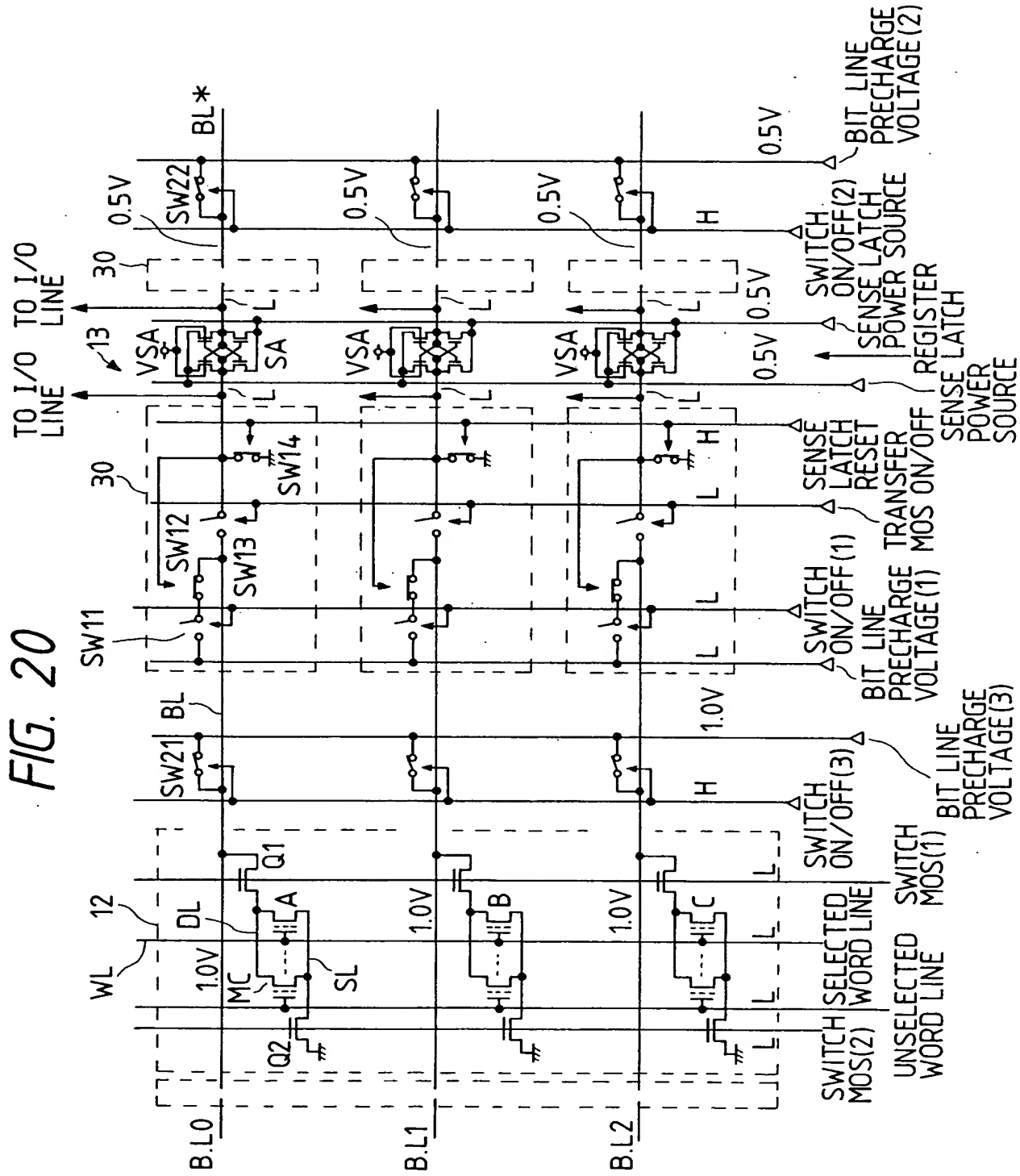

TO I/O LINE
TO I/O LINE
13
30
30
SW11
SW12
SW13
SW14
SW21
SW22
BL
BL*
VSA
SA
WL
12
DL
MC
Q1
Q2
A
B
C
SL
1.0V
0.5V
H
L
B.L0
B.L1
B.L2
SWITCH ON/OFF(1)
BIT LINE PRECHARGE VOLTAGE(1)
SENSE LATCH RESET TRANSFER MOS ON/OFF
SENSE LATCH POWER SOURCE REGISTER
SWITCH ON/OFF(2)
SENSE LATCH POWER SOURCE
BIT LINE PRECHARGE VOLTAGE(2)
SWITCH ON/OFF(3)
BIT LINE PRECHARGE VOLTAGE(3)
SWITCH MOS(1)
SELECTED WORD LINE
SWITCH MOS(2)
UNSELECTED WORD LINE

FIG. 21

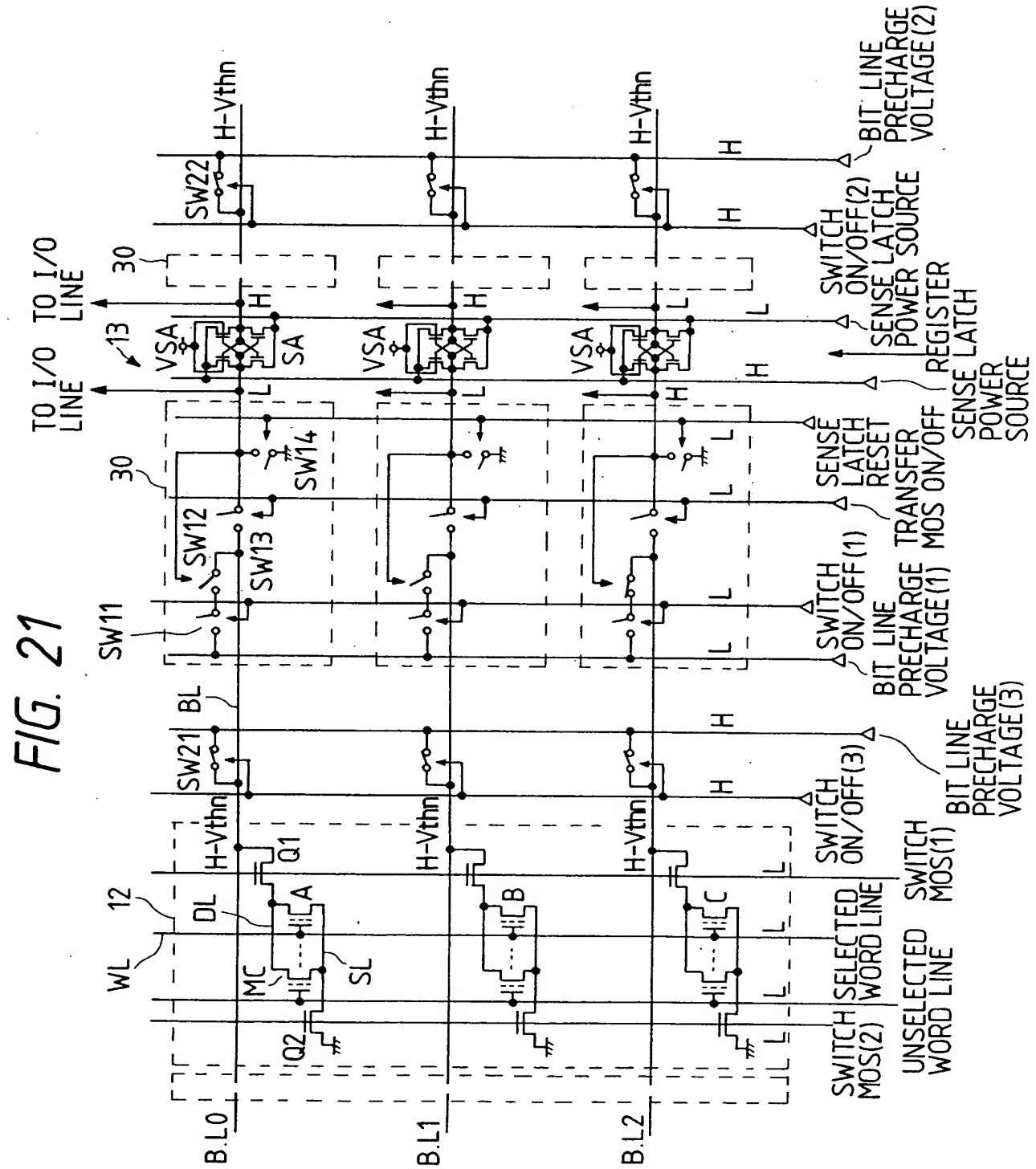

TO I/O LINE
TO I/O LINE
13
30
30
SW11
SW12
SW13
SW14
SW21
SW22
BL
VSA
SA
H-Vthn
Q1
Q2
MC
DL
WL
12
SL
A
B
C
B.L0
B.L1
B.L2
SWITCH MOS(2)
SELECTED WORD LINE
UNSELECTED WORD LINE
SWITCH MOS(1)
SWITCH ON/OFF(3)
BIT LINE PRECHARGE VOLTAGE(3)
SWITCH ON/OFF(1)
BIT LINE PRECHARGE VOLTAGE(1)
SENSE LATCH RESET
TRANSFER MOS ON/OFF
SENSE LATCH POWER SOURCE
REGISTER SENSE LATCH POWER SOURCE
SWITCH ON/OFF(2)
BIT LINE PRECHARGE VOLTAGE(2)
H
L

FIG. 22

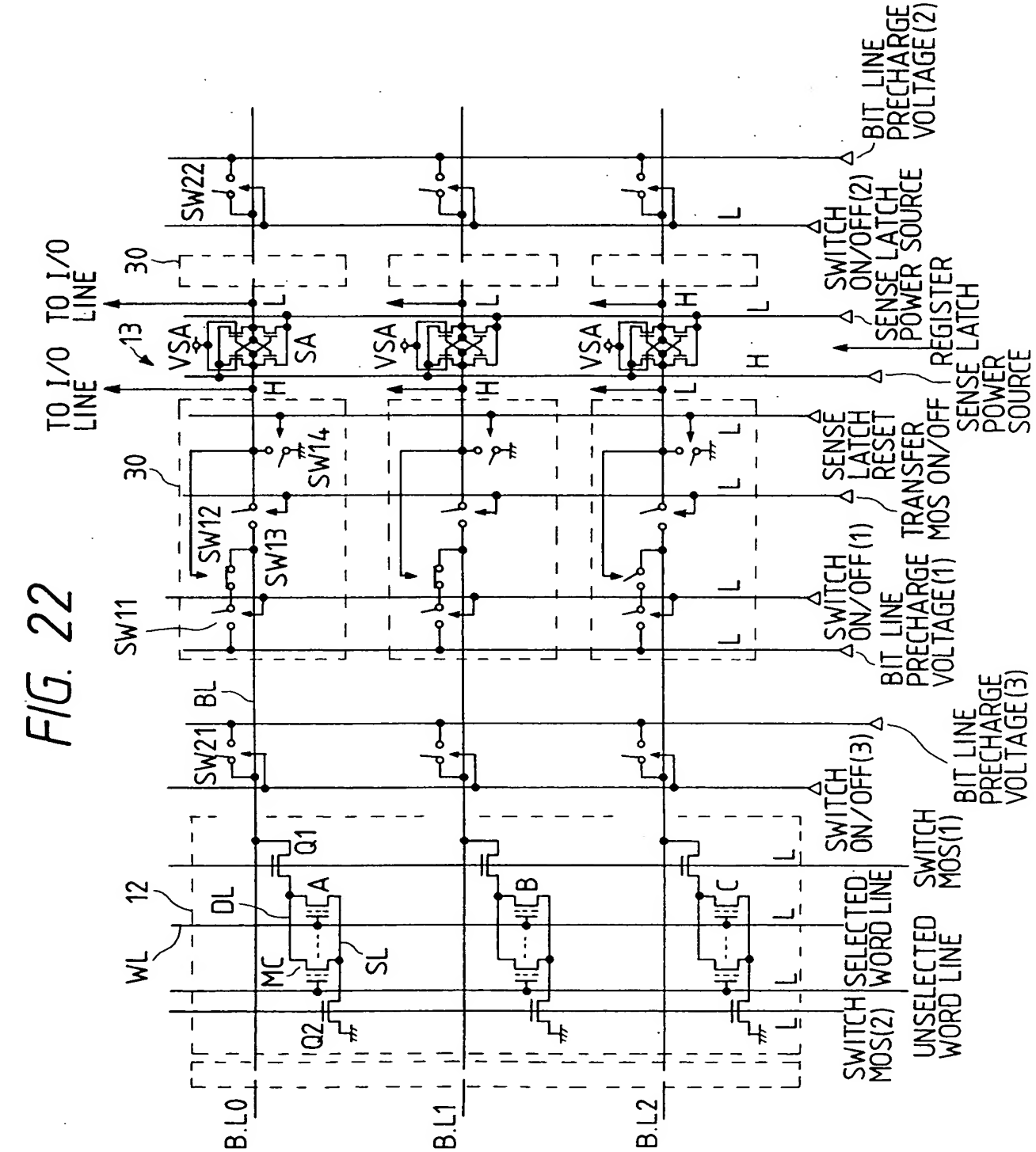
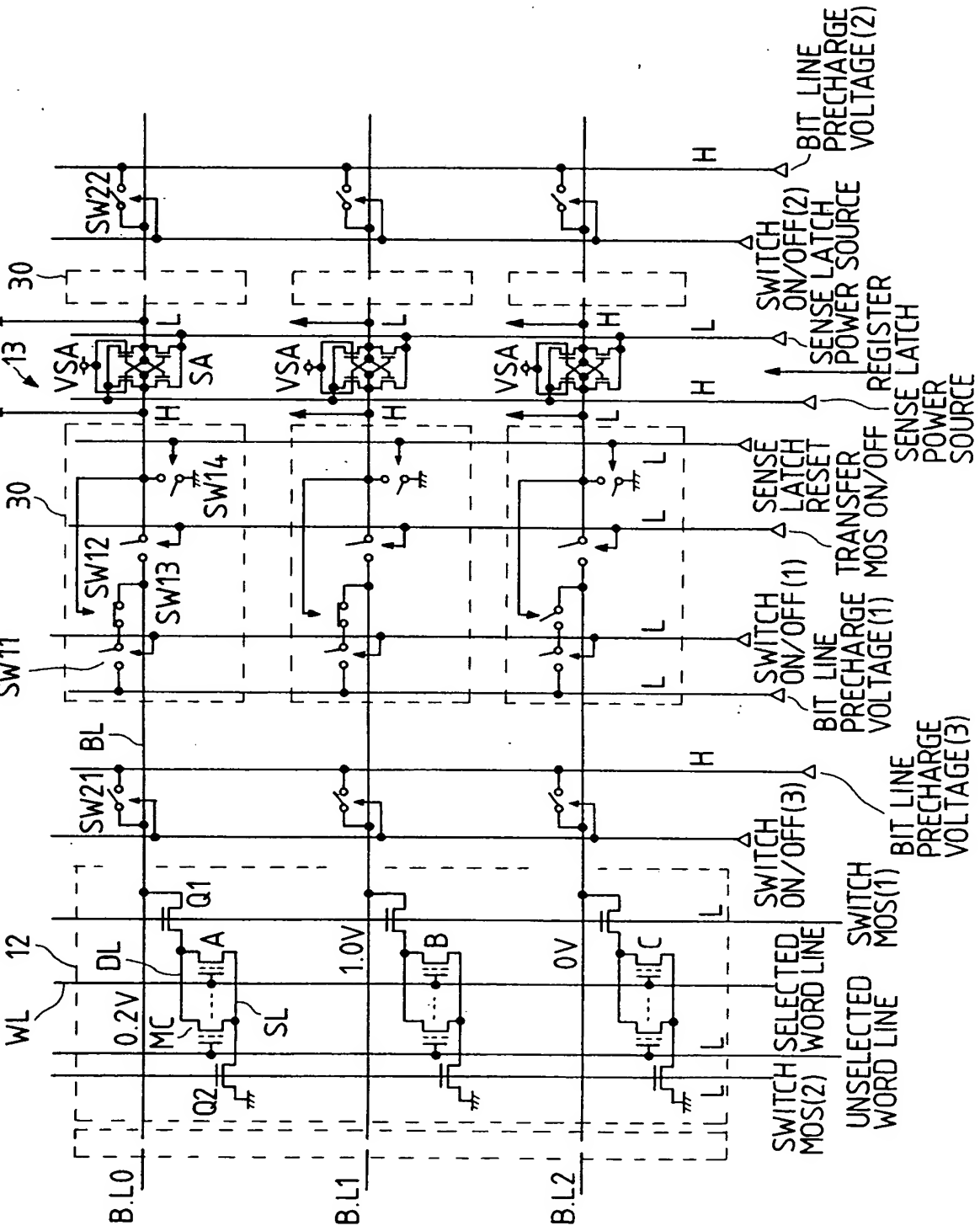

TO I/O LINE
TO I/O LINE
13
30
30
SW22
SW14
SW12
SW13
SW11
SW21
BL
VSA
SA
H
L
WL
12
DL
MC
SL
Q1
Q2
A
B
C
B.L0
B.L1
B.L2
SWITCH ON/OFF(2)
SENSE LATCH POWER SOURCE
BIT LINE PRECHARGE VOLTAGE(2)
REGISTER SENSE LATCH POWER SOURCE
SENSE LATCH RESET
TRANSFER MOS ON/OFF
SWITCH ON/OFF(1)
BIT LINE PRECHARGE VOLTAGE(1)
SWITCH ON/OFF(3)
BIT LINE PRECHARGE VOLTAGE(3)
SELECTED WORD LINE
SWITCH MOS(1)
SWITCH MOS(2)
UNSELECTED WORD LINE

FIG. 23


TO I/O LINE
TO I/O LINE
13
30
VSA
SA
SW11
SW12
SW13
SW14
SW21
SW22
BL
WL
12
DL
MC
Q1
Q2
A
B
C
SL
0.2V
1.0V
0V
B.L0
B.L1
B.L2
SELECTED WORD LINE
UNSELECTED WORD LINE
SWITCH MOS(1)
SWITCH MOS(2)
SWITCH ON/OFF(1)
SWITCH ON/OFF(2)
SWITCH ON/OFF(3)
BIT LINE PRECHARGE VOLTAGE(1)
BIT LINE PRECHARGE VOLTAGE(2)
BIT LINE PRECHARGE VOLTAGE(3)
SENSE LATCH RESET
TRANSFER MOS ON/OFF
SENSE LATCH POWER SOURCE
REGISTER SENSE LATCH POWER SOURCE
H
L